REMARKS/ARGUMENTS

Claims 1-4, 6, 8-14, and 16-17 are pending in the application and stand rejected.

Claims 12 and 16 are rejected under 35 USC 102 as being anticipated by United States Patent No. 7,065,072 to Quiles et al. (hereinafter "Quiles").

Claims 1-3, 6, 8, 11, and 17 are rejected under 35 USC 103 as being unpatentable over Quiles in view of United States Patent No. 6,597,689 to Chiu et al. (hereinafter "Chiu").

Claims 4 and 9-10 are rejected under 35 USC 103 as being unpatentable over Quiles in view of Chiu and further in view of United States Patent Application Publication No. 2001/0037435 to Van Doren.

Claims 1, 6, and 12 are amended. Support for the claim amendments can be found throughout the application. Among other places, support can be found at paragraphs [24]-[26] and with reference to Figs. 2-4. No new matter has been added.

As discussed below, Applicants respectfully submit that the cited references fail to anticipate or render obvious the pending claims. Quiles does not disclose at least first and second control processors or that such control processors manage first and second logical nodes, respectively, as these limitations are recited in claim 12. Secondary references Chiu and Van Doren fail to cure these and other deficiencies relating to independent claims 1 and 6. Reconsideration and allowance of all pending claims in view of the preceding amendments and the following remarks is respectfully requested.

Rejections under Section 102

A. Claim 12

Claim 12 recites a method of routing packets comprising a first logical node and a second logical node. The method includes "managing routing paths within the first logical node with a first control processor distinct from the first set of data processors; managing routing paths within the second logical node with a second control processor distinct from the second set of data processors; receiving data associated with a first network service provider; routing the data between data processors of the first logical node according to a first mapping of the first

control processor; receiving data associated with a second network service provider; and routing the data between data processors of the second logical node according to a second mapping of the second control processor." Quiles does not disclose or fairly suggest at least these claimed features.

Quiles discusses a digital subscriber line access multiplexer (DSLAM) which forms part of the local loop connecting home users with a central office. According to Quiles, the DSLAM permits various competitive local exchange carriers to connect their lines to different ports so that they can compete with the incumbent local exchange carrier to provide DSL service. See, Quiles at col. 4, ll. 27-36.

Referring to Fig. 2, the Examiner argues that line cards 74, 76 teach the claimed first and second data processors and that Quiles discloses logical nodes as being those cards which belong to a particular service provider. See, Office Action at ¶¶1,8. The Examiner also maintains that Quiles teaches the claimed first and second control processors through network interface (NIC) elements 66, 68. Id. Applicants respectfully disagree.

Assuming, for the sake of argument, that Quiles' network interface cards could be regarded as control processors, it is clear from the reference that only one such control processor routes data for all line cards. Network interface card 66 transports data between line cards 87 and network 18 and is common to all service providers. See, Quiles at col. 4, ll. 41-45. Network interface card 68 is merely a backup for redundancy and can be omitted without affecting the exchange of data. See, Quiles at col. 4, ll. 56-59. Thus, even under the assumption that NICs 66,68 are control processors, Quiles does not disclose "managing routing paths within the first logical node with a first control processor distinct from the first set of data processors; managing routing paths within the second logical node with a second control processor distinct from the second set of data processors."

In addition, unlike claim 12, Quiles does not disclose or fairly suggest routing data between data processors configured as a logical node. As discussed in the reference, line cards 87 are DSL modems which are associated with specific DSL customers. See, Quiles at col. 5, ll. 1-3. Quiles does not teach or suggest routing data *between* DSL modems ("data processors"), nor does it disclose managing routing paths within a collection of DSL modems

("logical nodes"). Accordingly, Applicants respectfully submit that Quiles does not disclose at least "receiving data associated with a first network service provider; routing the data between data processors of the first logical node according to a physical-to-logical mapping of the first control processor; receiving data associated with a second network service provider; and routing the data between data processors of the second logical node according to a physical-to-logical mapping of the second control processor."

B. Claim 16

Claim 16 depends from claim 12 and incorporates all of its limitations. As such, claim 16 is believed allowable over Quiles for at least the reason that it depends from an allowable base claim. In addition, claim 16 recites "wherein the first control processor manages data routing paths for the first network service provider and the second control processor manages data routing paths for the second network service provider." As previously discussed, Quiles does not disclose or suggest first and second control processors which manage data routing paths for first and second service providers.

Rejections under Section 103

A. Claim 1

Claim 1 recites a telecommunications device comprising "a plurality of control processors, each control processor configured to manage data routing paths between data processors in the plurality of data processors according to the corresponding physical locations of the data processors in the telecommunications device; and a plurality of logical nodes, wherein each logical node includes one or more data processors in the telecommunications device and is associated with a control processor in the plurality of control processors such that each control processor is coupled to a first data processor of its associated logical node and manages data routing paths for the logical node in relation to said first data processor." Quiles in view of Chiu does not teach or suggest a telecommunications device with at least these limitations.

As discussed in connection with claim 12, Quiles does not disclose a plurality of control processors configured to manage data routing paths. Nor does Quiles disclose or fairly suggest data routing paths between data processors in a logical node. Chui does not cure these deficiencies. In the portion cited by the Examiner, Chiu discusses that a chassis switch card passes data to line cards according to a virtual path identifier. See, Chiu at col. 26, ll. 26-37. Chui does not disclose or suggest data routing paths *between* line cards. See e.g., Fig. 5. Chiu also fails to disclose that line cards are arranged into logical nodes or that a control processor is associated with each logical node. Further, Chui fails to disclose that, for each logical node, a control processor manages data routing paths in relation to a first data processor. Accordingly, Applicants respectfully submit that Quiles in view of Chiu fails to teach or suggest each and every element as claimed.

B. Claim 6

Claim 6 recites limitations similar to those discussed in connection with claim 1 and is believed allowable over the cited references for at least the reasons previously given. In particular, claim 6 recites a logical shelf comprising "a first control processor separate from the first set of data processors configured to manage data routing paths between data processors of the first set according to their corresponding positions in the first logical shelf, and a second control processor separate from the second set of data processors configured to manage data routing paths between data processors of the second set according to their corresponding positions in the second logical shelf." Quiles in view of Chiu does not disclose or fairly suggest at least a logical shelf as claimed.

C. Dependent claims

Claims 2-4, 8-11, and 13-17 depend from claims 1, 6, and 12, respectively. Each dependent claim incorporates all of the limitations of its respective base claim and each is therefore believed allowable for at least the reason that it depends from an allowable base claim in addition to being allowable based on its additional limitations. Reconsideration and allowance of all pending claims is respectfully requested.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 858-350-6100.

Respectfully submitted,

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